1. A method for fabricating a plurality of capacitors comprising:

providing a plurality of contact plugs through an insulating layer to semiconductor device structures in a substrate wherein said contact plugs are formed in a logic area of said substrate and in a memory area of said substrate and providing a plurality of node contact plugs to node contact regions within said substrate in said memory area; and

thereafter fabricating a plurality of capacitors wherein each said capacitor contacts one of said node contact plugs and wherein said capacitors are fabricated in a twist line pattern in a self-aligned copper process.

2. The method according to Claim 1 wherein said step of fabricating said plurality of capacitors comprises:

depositing a silicon carbide layer overlying said contact plugs;

depositing a low dielectric constant material layer overlying said silicon carbide layer;

depositing a stop layer overlying said low dielectric constant material layer;

forming a first openings through said stop layer, said low dielectric constant material layer, said

silicon carbide layer, and said insulating layer to said node contact plugs;

depositing a first metal layer overlying said stop layer and within said first openings;

filling said first openings with a sacrificial layer;

etching a twisted trench by etching back said sacrificial layer and said first metal layer to leave said first metal layer only within said first openings and recessed from the top of said first openings wherein said first metal layer forms bottom electrodes of said capacitors;

thereafter removing said sacrificial layer;

depositing a capacitor dielectric layer overlying said bottom electrodes;

depositing a second metal layer overlying said capacitor dielectric layer;

depositing a third metal layer overlying said second metal layer and filling said first openings; and

polishing back said third metal layer, said second metal layer, and said capacitor dielectric layer to leave these layers only within said first openings wherein said second and third metal layers together form top electrodes of said capacitors.

3. The method according to Claim 1 wherein said twist line pattern comprises:

two twisted trenches that are mirror images of each other wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance.

4. The method according to Claim 1 wherein said semiconductor structures include gate electrodes and associated source and drain regions.

5. The method according to Claim 1 wherein said contact plugs comprise tungsten.

6. The method according to Claim 2 wherein said first and second metal layers comprise tantalum nitride or titanium nitride.

7. The method according to Claim 2 wherein said third and fourth metal layers comprise copper.

8. The method according to Claim 2 wherein said sacrificial layer comprises photoresist.

9. The method according to Claim 1 after said step of removing said sacrificial layer further comprising:

etching additional openings between said bottom electrodes through said insulating layer to said stop layer to increase capacitor area.

10. The method according to Claim 2 wherein said capacitor dielectric layer comprises a high dielectric constant material and has a thickness of between about 100 and 400 Angstroms.

11. The method according to Claim 2 wherein said capacitor dielectric layer comprises tantalum oxide (Ta_2O_5).

12. The method according to Claim 3 further comprising:

etching second openings to said contact plugs in said logic area and in said memory area wherein said second opening in said memory area lies between said two twisted trenches and in a horizontal line with one capacitor pair wherein said one capacitor pair has said first separation distance and adjacent capacitor pairs

have said second separation distance; and

filling said second openings with a metal layer to complete contacts to said contact plugs in said logic area and in said memory area.

13. A method for fabricating a plurality of capacitors comprising:

providing a plurality of contact plugs through an insulating layer to semiconductor device structures in a substrate wherein said contact plugs are formed in a logic area of said substrate and in a memory area of said substrate and providing a plurality of node contact plugs to node contact regions within said substrate in said memory area;

thereafter fabricating a plurality of capacitors wherein each said capacitor contacts one of said node contact plugs and wherein said capacitors are fabricated in a twist line pattern in a self-aligned copper process comprising:

providing first openings through an insulating layer to said node contact plug;

depositing a first metal layer within said first openings;

forming a twisted trench by etching back said first metal layer to leave said first metal layer only within

said first openings and recessed from the top of said first openings wherein said first metal layer forms bottom electrodes of said capacitors;

depositing a capacitor dielectric layer overlying said bottom electrodes;

depositing a second metal layer overlying said capacitor dielectric layer and filling said first openings to form top electrodes of said capacitor;

etching second openings through said insulating layer to said contact plugs; and

filling said second openings with a third metal layer to complete contacts to said contact plugs in said logic area and in said memory area.

14. The method according to Claim 13 wherein said step of providing first openings through an insulating layer to said node contact plug comprises:

depositing a silicon carbide layer overlying said contact plugs;

depositing a low dielectric constant material layer overlying said silicon carbide layer;

depositing a stop layer overlying said low dielectric constant material layer; and

forming first openings through said stop layer, said low dielectric constant material layer, said

silicon carbide layer, and said insulating layer to said node contact plug.

15. The method according to Claim 13 wherein said semiconductor structures include gate electrodes and associated source and drain regions.

16. The method according to Claim 13 wherein said twist line pattern comprises:

two twisted trenches that are mirror images of each other wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance.

17. The method according to Claim 13 wherein said contact plugs comprise tungsten.

18. The method according to Claim 13 wherein said first and second metal layers comprise tantalum nitride.

19. The method according to Claim 13 wherein said third

and fourth metal layers comprise copper.

20. The method according to Claim 13 wherein said sacrificial layer comprises photoresist.

21. The method according to Claim 13 after said step of removing said sacrificial layer further comprising:

etching additional openings between said bottom electrodes through said insulating layer to said stop layer to increase capacitor area.

22. The method according to Claim 13 wherein said capacitor dielectric layer comprises a high dielectric constant material and has a thickness of between about 100 and 400 Angstroms.

23. The method according to Claim 13 wherein said capacitor dielectric layer comprises tantalum oxide (Ta_2O_5).

24. The method according to Claim 15 wherein in said step of etching second openings to said contact plugs, said second opening in said memory area lies between said two twisted trenches and in a horizontal line with one capacitor pair wherein said one capacitor pair has

said first separation distance and adjacent capacitor pairs have said second separation distance.

25. A method for fabricating a plurality of capacitors comprising:

providing a plurality of contact plugs through an insulating layer to semiconductor device structures in a substrate wherein said contact plugs are formed in a logic area of said substrate and in a memory area of said substrate and providing a plurality of node contact plugs to node contact regions within said substrate in said memory area;

thereafter fabricating a plurality of capacitors wherein each said capacitor contacts one of said node contact plugs and wherein said capacitors are fabricated in a twist line pattern in a self-aligned copper process wherein said twist line pattern comprises two twisted trenches that are mirror images of each other wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance and wherein said process comprises:

depositing a silicon carbide layer overlying said contact plugs;

depositing a low dielectric constant material layer overlying said silicon carbide layer;

depositing a stop layer overlying said low dielectric constant material layer;

forming first openings through said stop layer, said low dielectric constant material layer, said silicon carbide layer, and said insulating layer to said node contact plug;

depositing a first metal layer overlying said stop layer and within said first openings;

filling said first openings with a sacrificial layer;

etching a twisted trench by etching back said sacrificial layer and said first metal layer to leave said first metal layer only within said first openings and recessed from the top of said first openings wherein said first metal layer forms bottom electrodes of said capacitors;

thereafter removing said sacrificial layer;

depositing a capacitor dielectric layer overlying said bottom electrodes;

depositing a second metal layer overlying said capacitor dielectric layer;

depositing a third metal layer overlying said second metal layer and filling said first openings;

polishing back said third metal layer, said second metal layer, and said capacitor dielectric layer to leave these layers only within said first openings wherein said second and third metal layers together form top electrodes of said capacitors;

etching second openings through said low dielectric constant layer and said silicon carbide layer to said contact plugs in said logic area and in said memory area wherein said second opening in said memory area lies between said two twisted trenches and in a horizontal line with one capacitor pair wherein said one capacitor pair has said first separation distance and adjacent capacitor pairs have said second separation distance; and

filling said second openings with a fourth metal layer to complete contacts to said contact plugs in said logic area and in said memory area.

26. The method according to Claim 25 wherein said semiconductor structures include gate electrodes and associated source and drain regions.

27. The method according to Claim 25 wherein said

contact plugs comprise tungsten.

28. The method according to Claim 25 wherein said first and second metal layers comprise tantalum nitride.

29. The method according to Claim 25 wherein said third and fourth metal layers comprise copper.

30. The method according to Claim 25 wherein said sacrificial layer comprises photoresist.

31. The method according to Claim 25 wherein said capacitor dielectric layer comprises a high dielectric constant material and has a thickness of between about 100 and 400 Angstroms.

32. The method according to Claim 25 wherein said capacitor dielectric layer comprises tantalum oxide (Ta_2O_5).

33. An embedded DRAM and capacitor structure device comprising:

trenched capacitors in two twisted trenches through an insulating layer in a memory area of an integrated circuit wherein said two twisted trenches are mirror

images of each other and wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance;

a bit line contact in said memory area through said insulating layer to a bit line wherein said bit line contact lies between said two twisted trenches and in a horizontal line with one capacitor pair wherein said one capacitor pair has said first separation distance and adjacent capacitor pairs have said second separation distance; and

first line metal contacts in a logic area of said integrated circuit;

wherein said bit line contact and said first line metal contacts are no higher vertically than said trenched capacitors.